**Design 4 bit ALU by using VHDL and verify its logical operation.**

entity alu\_1 is

Port ( A : in STD\_LOGIC\_VECTOR (3 downto 0);

B : in STD\_LOGIC\_VECTOR (3 downto 0);

SEL : in STD\_LOGIC\_VECTOR (3 downto 0);

Y : out STD\_LOGIC\_VECTOR (3 downto 0));

end alu\_1;

architecture Behavioral of alu\_1 is

begin

**process(A,B,SEL)**

**begin**

**case SEL is**

**when "0000" => Y <= A and B;**

**when "0001" => Y <= A nand B;**

**when "0010" => Y <= A or B;**

**when others => NULL; [[ i.e. when others => Y <= (others => 'Z');]]**

**end case;**

**end process;**

end Behavioral;

**Test bench for ALU 4 bit**

stim\_proc: process

begin

**A<="0101"; B<="0101";**

SEL <="0000"; wait for 100 ns;

SEL <="0001"; wait for 100 ns;

SEL <="0010"; wait for 100 ns;

**A<="1101"; B<="1101";**

SEL <="0000"; wait for 100 ns;

SEL <="0001"; wait for 100 ns;

SEL <="0010"; wait for 100 ns;

wait;

end process;

END;

